

improved linearity.

Capacitor C7 and resistor R8 compensate the operational amplifier 18, against oscillation in the linear region of operation. The values chosen for resistors R7 and R9 insure deep saturation of the FET 22, while protecting the gate voltage rating.

Since other modifications and changes varied to fit particular operating requirements and environments will be apparent to those skilled in the art, the invention is not considered limited to the example chosen for purposes of disclosure, and covers all changes and modifications which do not constitute departures from the true spirit and scope of this invention.

Having thus described the invention, what is desired to be protected by Letters Patent is presented in the subsequently appended claims.

What is claimed is:

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1 1. An inrush circuit for electronic devices having
2 high input capacitance, said inrush circuit comprising:

3 time delay means for eliminating false action;

4 means for providing a voltage ramp, operatively
5 connected to said time delay means;

6 means defining an output voltage;

7 an operational amplifier circuit having a
8 reference input, said operational amplifier
9 circuit receiving said voltage ramp at said
10 reference input and comparing a divided sample
11 of said output voltage with the voltage ramp, said
12 operational amplifier operating in a linear
13 mode, whereby said output voltage approximates a
14 multiple of the voltage ramp; and

15 transistor means electronically connected to said
16 operational amplifier circuit, said transistor
17 means operating in linear mode during capacitor
18 charging, and subsequently reaching a full-ON

19 state, in order to convey full power supply
20 capacity to a load during normal operation.

1 2. The inrush circuit for electronic devices in
2 accordance with claim 1, wherein said transistor means
3 comprises a power field effect transistor.

1 3. The inrush circuit for electronic devices in
2 accordance with claim 1, wherein said output voltage
3 approximates the voltage ramp by a gain of two.

1 4. The inrush circuit for electronic devices in
2 accordance with claim 1, wherein said electronic devices
3 comprise a point-of-sale printer.

1 5. The inrush circuit for electronic devices in
2 accordance with claim 1, wherein said time delay means
3 reaches threshold in approximately 50 ms.

1 6. The inrush circuit for electronic devices in
2 accordance with claim 2, wherein said field effect
3 transistor is operative initially in an OFF state, and
4 subsequently becomes operative in a full-ON state.

1 7. The inrush circuit for electronic devices in
2 accordance with claim 6, wherein said field effect
3 transistor is part of a linear feedback loop, and further
4 comprising capacitive means electronically connected to said
5 field effect transistor for ensuring that said field effect
6 transistor is initially operative in said OFF state, said
7 capacitive means being minimized to subsequently prevent
8 interfering with said linear feedback loop.

1 8. The inrush circuit for electronic devices in
2 accordance with claim 2, further comprising capacitive means
3 electronically connected to said operational amplifier for
4 preventing oscillation thereof.

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1 9. An inrush circuit for electronic devices having
2 high input capacitance, said inrush circuit comprising:

3 means for providing a voltage ramp;

4 means defining an output voltage;

5 an operational amplifier circuit having a
6 reference input, said operational amplifier
7 circuit receiving said voltage ramp at said
8 reference input and comparing a divided sample
9 of said output voltage with the voltage ramp, said
10 operational amplifier operating in a linear
11 mode, whereby said output voltage approximates a
12 multiple of the voltage ramp; and

13 a field effect transistor electronically connected
14 to said operational amplifier circuit, said
15 field effect transistor operating in linear mode
16 during capacitor charging, and subsequently
17 reaching a full-ON state in order to convey full
18 power supply capacity to a load during normal
19 operation.

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1 10. The inrush circuit for electronic devices in
2 accordance with claim 9, wherein said output voltage
3 approximates the voltage ramp by a gain of two.

1 11. The inrush circuit for electronic devices in
2 accordance with claim 9, wherein said electronic devices
3 comprise a point-of-sale printer.

1 12. The inrush circuit for electronic devices in
2 accordance with claim 9, wherein said time delay means
3 reaches threshold in approximately 50 ms.

1 13. The inrush circuit for electronic devices in
2 accordance with claim 9, wherein said field effect
3 transistor is operative initially in an OFF state, and
4 subsequently becomes operative in a full-ON state.

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1 14. The inrush circuit for electronic devices in
2 accordance with claim 13, wherein said field effect
3 transistor is part of a linear feedback loop, and further
4 comprising capacitive means electronically connected to said
5 field effect transistor for ensuring that said field effect
6 transistor is initially operative in said OFF state, said
7 capacitive means being minimized to subsequently prevent
8 interfering with said linear feedback loop.

1 15. The inrush circuit for electronic devices in
2 accordance with claim 9, further comprising capacitive means
3 electronically connected to said operational amplifier, for
4 preventing oscillation thereof.

1 16. The inrush circuit for electronic devices in
2 accordance with claim 9, further comprising time delay means
3 electronically connected to said means for providing said
4 voltage ramp, said time delay means eliminating false
5 action.